Listing of the Claims:

This listing of claims reflects the claims currently pending in the present application.

1-37. (Cancelled)

38. (Previously presented) An in-process substrate structure including a plurality of contact regions and a plurality of non-contact regions adjacent the contact regions on a surface of the substrate, the in-process substrate structure comprising:

a selectively formed contact on each contact region, each contact being isolated from contacts on adjacent contact regions and having a first surface exposed to electromagnetic radiation during formation to a greater extent than a second surface of the contact.

39-44. (Cancelled)

45. (Previously presented) The substrate of claim 38 wherein the non-contact regions adjacent to the contact region comprise isolation oxide regions.

46. (Previously presented) The substrate of claim 38 wherein the substrate comprises silicon.

47. (Previously presented) The substrate of claim 38 wherein the substrate comprises gallium arsenide.

48. (Previously presented) The substrate of claim 38 wherein the substrate comprises silicon germanium.

49. (Previously presented) The substrate of claim 38 wherein the contact comprises silicon.

50. (Previously presented) The substrate of claim 38 wherein the contact comprises gallium arsenide.

51. (Previously presented) The substrate of claim 38 wherein the contact comprises silicon germanium.

52. (Previously presented) An in-process semiconductor structure, comprising:

a substrate;

a plurality of active regions;

a plurality of isolation regions adjacent the active regions, each isolation region being positioned between adjacent active regions to isolate adjacent active regions; and

at least one selectively formed contact region on each active region, each selectively formed contact region being isolated from contacts on adjacent active regions and having a first surface exposed to electromagnetic radiation during formation to a greater extent than a second surface of the contact.

53. (Previously presented) The in-process semiconductor structure of claim 52 wherein each isolation region comprises a field oxide region.

54. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises silicon.

55. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises gallium arsenide.

56. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises silicon germanium.

57. (Previously presented) The in-process semiconductor of claim 53 wherein each contact comprises selective epitaxial growth silicon.

58. (Previously presented) The in-process semiconductor of claim 53 wherein at least some of the contacts comprise gallium arsenide.

59. (Previously presented) The in-process semiconductor of claim 53 wherein at least some of the contacts comprise silicon germanium.

60. (Previously presented) The substrate of claim 38 wherein the electromagnetic radiation comprises collimated electromagnetic radiation.

61. (Previously presented) The in-process semiconductor of claim 53 wherein the electromagnetic radiation comprises collimated electromagnetic radiation.